

Single-Phase Transformer-less Inverter Circuit Configurations for Photovoltaic Applications

*R. Selvamathi*¹ and V. Indragandhi² ¹Research Scholar, SENSE, VIT, Vellore (Tamil Nadu), India. ²Associate Professor, SELECT, VIT, Vellore (Tamil Nadu), India.

(Corresponding author: V. Indragandhi) (Received 17 October 2019, Revised 09 December 2019, Accepted 18 December 2019) (Published by Research Trend, Website: www.researchtrend.net)

ABSTRACT: Grid-connected inverters are the critical components of distributed generation system because of their function as an efficient interface between renewable energy sources and utility. Recently, there has been an increasing interest in the use of Transformerless Inverter (TI) for low voltage single phase gridconnected Photovoltaic (PV) system due to high efficiency, low cost, small size, and weight compared to those with a transformer. This research review emphases on the TI topologies, which are categorized into four primary groups based on the structure, leakage current, and device characteristics. Various configurations like H5, H6, Highly Efficient and Reliable Inverter Concept (HERIC) and Neutral-Point Clamped (NPC) are offered, associated and analyzed based on leakage current in the topology, component count and ratings, benefits and difficulties.

Keywords: Device Characteristics, HERIC, Leakage current, Photovoltaic systems, Transformer-less Inverter.

Abbreviations: TI, transformerless inverter; HERIC, highly efficient and reliable inverter concept; PV, photo voltaic; NPC, neutral point clamped.

I. INTRODUCTION

An inverter can be either non-isolated or isolated which depends on the decoupling between the utility grid and PV panels. The galvanic isolation is often identified with the transformer. It has a major influence on the grid-connected PV system based on DC to AC conversion efficiency. For such systems, isolation entirely depends on the regulations of the country. Galvanic isolation is a requirement for different countries such as Italy, United Kingdom, etc. and is done in two ways. First, as the high-frequency transformer on the converter's DC side or as by the low-frequency step-up transformer on the grid side. It can be seen in Fig. 1 and 2 respectively.



Fig. 1. High-Frequency Transformer.



Fig. 2. Low-Frequency Transformer.

On the contrary, galvanic isolation can be excluded in some countries like Spain and Germany. If it is left out, to separate the electrical grid and PV array, another technological solution is used. Fig. 3 shows the details of the PV system without transformer, which reduces the size, cost, and weight of the whole PV system. In transformer less systems, the main problem is that sometimes it causes DC to be injected into AC by the inverter [1-3]. So, in the distribution transformer, it can saturate the magnetic core which results in overheating of the system and may lead to potential failure. One of the main advantages of these types of systems is that they can increase the system's overall efficiency [4-6].



Fig. 3. Transformer less Inverter.

By using the database having the information about more than 400 commercially presented PV system provided by a magazine of PV business, Fig. 4 has been used to explain the maximum efficiency of these systems. Dots (o) has been used to represent the TIs, (*) represent the

low-frequency transformer inverters along with the galvanic isolation between the Grid and the PV and (Δ) triangles represents the high DC-DC topologies. In this figure, we can see that if the PV system is up to 6.5 kW, the maximum efficiency of inverters with galvanic isolation can go to 96-96.5%. While the maximum capabilities of TIs can be reached to 98%. We can see that maximum TI has high efficiency. Along with high efficiency, TI has less weight, size as compare to the galvanic separation [7].



Fig. 4. PV Inverter Comparison, based on PHOTON database [38].

For solar PV based decentralized grid, the TI topologies are becoming very famous in recent years. The main reason for that is they are cheaper, have less weight, small size and are more efficient. Due to this, they are preferred. But the problem is that TI does not have galvanic isolation to decouple the PV array and the grid which might cause the leakage of the current within parasitic capacitance and it is located between the ground and the PV panel. Due to this, TI has problems such as additional power loss, electromagnetic radiation. It also raises some safety issues as well. A lot of research has been done to overcome this problem, and the research can be classified into three groups which are (a) Topologies of H-bridge based inverter, (b) neutral point clamp inverter topologies and (c) HERIC topologies. This review paper is organized as follows: Section II reviews about the H5 TI topologies, H6 inverter topologies are mentioned in the section III, HERIC inverter topologies are explained in the section IV followed by NPC schemes in section V and section VI deals about comparative study on various topologies. In section VII concludes this review paper.

II. H5 INVERTER CONFIGURATIONS

In this section H5 inverter topologies available in the literature and common mode voltage obtained from Simulink circuits is discussed. In Fig. 5 the H5 topology which is a full bridge and it consists of five switches which are S1, S2, S3, S4 and S5 switch from the DC bypass. Moreover, the grid frequency is used to operate the switches S1 and S2. The other three switches are operated at the high frequency. If the switch S5 is open in the free-wheeling period, it disconnects the inverter full H-bridge from the PV panel. Especially for the partial load, H5 TI topology usage helps us to gain high efficiency. In a comparison of full H-bridge topology, it only needs one extra transistor. If the best suitable semiconductor is not chosen in H-Bridge inverter, the transistor is in series which might increase the conduction losses [8].



Fig. 5. H5 Circuit Topology 1.

Fig. 6 displays another TI topology called H5 topology which has been proposed in [8]. In this topology, another switch is added to the Fly-Back (FB) inverter's DC side. The body diode of S3 and switch S1 is responsible for the freewheeling current flow. Due to the low reverse recovery of the MOSFET body diode, switch S1 and S3 cannot be implemented in this topology using MOSFET. Another disadvantage of this system is that, in active mode for the complete grid cycle, the current flows via three switches. This results in more conduction losses. Common Mode (CM) voltage is fluctuating as at the midpoint of DC link; the freewheeling current path potential is not fixed.





Different advantages offered by this presented topology are (1) By using SiC and MOSFETs diodes, it provides high efficiency for high load range (2) During all operations, the CM voltage is constant which results in low leakage current because the clamping branch is added (3) With unipolar Sinusoidal Pulse Width Modulation (SPWM), it achieves excellent Differential Mode (DM) characteristics like the isolated FB inverter (4). for main power switches, Pulse Width Modulation (PWM) dead time is not required. It results in low distortion at the output [9-10].

The H5 topology is made up of a full bridge along with an extra switch in the DC link. Through the freewheeling period of the current, it helps to decouple the gird from the PV inverter. Due to this, the current has a switching ripple effect which is equivalent to the grid switching frequency. Due to this ripple effect, it requires high filtering effort. Low core losses are expected because of the unipolar voltage across the filter.



Fig. 7. SiC-based H5 Topology.



Fig. 8. Si and SiC-based Inverter Comparison.

By considering the energy production, the optimized SiCbased H5 TIs are proven to more efficient and effective compared to the non-optimal and Si-based as counterparts. Even at higher switching frequencies, they can work efficiently, and it has less cost, weight, and size as compared to PV inverter output filter. It can be seen in Fig. 7. It shows that SiC type power semiconductors price is reducing in the market as compared to the level of different Si-based technology. It serves as one of the most crucial factors to develop and produce optimized SiC-based PV inverter which has a low cost of energy in contrast to the other PV inverters which are using Si Technology. Not only that they are efficient, but they also provide maximum economics profitability. The comparison of Si and SiC based inverter presented in Fig. 8 which is designed with L-Lg-Cf-Lf filter [11-13]. Output voltage and common voltage of H5 topology is shown in Fig. 9 (a) and (b). The reason for that is the voltage to ground VPE is sinusoidal with grid frequency component [14-16].



Fig. 9 (a) H5 Topology output Voltage.



Fig. 9 (b) H5 Topology Common mode Voltage.

III. H6 TI INVERTER CONFIGURATIONS

In this section H6 inverter topologies available in the literature and common mode voltage obtained from Simulink circuits is discussed. H6 inverter with the six switches which are S1-S6 is shown in Fig. 10. Filter device which is connected to the grid consists of L₁, L₂, C₁ and input capacitor is C_{dc}. u_{AN} and u_{BN} the potential between the middle point A and B to the terminal N, respectively. UPV represents the input voltage. Another switch S6 is introduced to increase the conversion efficiency. It introduces a new power path in the structure and this topology presents the excellent trade-off between the common-mode performance and power loss, and it is better than with H5 [17-18].



Fig. 10. H6 Topology 1.

H6-type configuration inverter circuit diagram is displayed in Fig. 11. It is composed of two freewheeling diodes, six power MOSFETs and two split inductors as a low-pass filter [19]. Due to the advantages explained below, this approach is suited for the non-isolated AC module. (1) As intrinsic body diodes are naturally not active, and MOSFETs are used for all active switches, it provides high efficiency on a varied load conditions. (2) As the voltage applied to the parasitic ground-loop capacitance has only low-frequency components, it has low ground leakage current. (3) It does not require any limited lifetime electrolytic capacitors for a split DC link as they are needed for the other half-bridge of inverters. (4) Fullbridge inverter with bipolar PWM switching has very high output inductance while this approach has smaller output inductance. (5) As no dead time is required in the proposed circuit, so there is Low output AC distortion. In same PWM cycle, same phase-leg active switches do not turn on [20-21].



Fig. 11. H6 Inverter Topology 2.

For non-isolated, PV AC module applications, a new and highly efficient topology is presented which uses MOSFETs for all active switches. H6-type configuration presented in [19, 22] have the following feature: low ground leakage current, over a wide load range it provides better efficiency, low-output AC-current distortion and split capacitors are not required Fig. 12.





H6-type PV inverter topology is presented in Fig. 13. MOSFETs are changed with Insulated-Gate Bipolar Transistors (IGBTs), and the other two diodes are removed. If we compare the result of the topology presented in Fig. 13, some differences between in control signals and the freewheeling path are automatically introduced. By using unipolar SPWM [23-25] some good CM and DM characteristics can be attained by using the prescribed topology [26-27].

(1) During the whole grid period, CM voltage is persistent, and leakage current is well suppressed even when reactive power is injected into the grid.

(2) In this topology, with unipolar modulation, excellent DM characteristics are acquired as it is an isolated fullbridge inverter.

(3) During the whole grid period, the inductor current flows through three switches, and the blocking voltages of the added switches are half of the DC input voltage. So due to this, the conduction losses and the switching losses are quite less.

(4) Reactive power can be injected into the utility grid in this topology, and it introduces very low harmonic distortion.

In Fig. 14, we can see a new approach for more efficient single-phase TI with hybrid modulation method. Inductors and power quality optimization is achieved due to the three-level output voltage in the inverter bridge's middle point (Fig.14). With H6-type configuration, leakage current issues and CM voltage in a non-isolated system is eliminated without input split capacitors. Output voltage and common voltage of H6 topology is shown in Fig. 15 (a), (b).



Fig. 13. H6 Inverter Topology 4.



Fig. 14. H6 Inverter Topology 5.



Fig. 15 (a) Output voltage of H6 inverter.





IV. HERIC TOPOLOGY

In this section HERIC inverter topologies available in the literature and common mode voltage obtained from Simulink circuits is discussed. Fig. 16 shows a HERIC inverter which is beneficial in both techniques which are bipolar modulation and unipolar modulation. Even though it has good performance, its commonality behavior as an H5 inverter takes a toll on its performance as not only has it a variable voltage in the common mode but also a high leakage of current in low efficiency. Providing galvanic isolation, H6 eliminates the common mode voltage clamping and leakage current, but overall efficiency of the system is reduced [28].



Fig. 16. HERIC Topology 1.

Two different alternate approaches are combined to use their advantages. First is the three-level output voltage of the unipolar PWM, as in the case of bipolar PWM, it reduces the CM voltage [29-31]. It consists of two switches and a full bridge inverter. It is demonstrated in Fig. 17. In the disconnection of PV array and the grid, switch S5 or S6 is used. It helps in reduction of the current leakage. Two added semiconductor devices are the main drawback of the proposed topology [32-34].



Fig. 17. HERIC Topology 2.

HERIC topology is one of the best transformerless topologies, and it is shown in Fig. 18. Sunway's converters are one of the commercial inverter switch have used this topology. During the freewheeling period to decouple the PV module from the grid, on AC side of a full-bridge topology, two switches are added. A CM voltage can be detected when the PV module is decoupled from the grid. It is because freewheeling path potential is not clamped which should be clamped at the half of dc input voltage.

Fig. 19 provides two different solutions to disconnect the DC source and the grid. For alternate use, two dotted blocks are added. Block one is added on the AC side and the other on the DC side of the converter. When a converter is used under unity power factor, it provides excellent performance. In the grid current freewheeling intervals, the AC or DC coupling allows the discontinuation of PV plants and the grid voltage.



Fig. 18. HERIC Topology 3.

Across the countries, it has been established as the worldwide standard that imposes the injection of some amount of reactive power when there are mandatory standards for the connection of grid-connected inverters [35]. This thing becomes a limitation of the provided solution.



Fig. 19. HERIC Topology 4.

The SMA H5 converter utilizes DC decoupling while the Sunways inverter named HERIC uses the AC decoupling. In each case, at the switching frequency of the converter, the output voltage is three level waveforms by using the necessary component. In this case, a current ripple has to take into account at set frequency in order to design output filter [36, 37].

Fig. 20 shows the traditional MOSFET-based phase legs of the TI. It shows a modification which ensures the high efficiency which replaces the IGBTs with MOSFETs and diodes and this change is shown in Fig. 20. A new family of new transformerless topologies is derived by combining these two-phase legs and is based on the AC separation and asymmetric phase legs. The following steps explain how to derive new topologies. (1) Switches used in HERIC which are IGBT are replaced with the diodes and MOSFETs to increase the efficiency (2) To derive a new topology, Combine these two-phase legs. Now by switching the places of freewheeling switches (D1 and S3), the new topologies are derived (3) Half the DC input voltage and clamp the CM voltage. Add a clamping branch consists of a diode and switch with a capacitor divider.



Fig. 20. HERIC Topology 5.



Fig. 21. HERIC Topology Proposed in [38].



Fig. 22. HERIC Topology Proposed in [39].

The simple H6 topologies are presented in Fig. 21 and 22. For transformerless PV grid-connected inverter; two key attributes are high efficiency and low leakage current. Due to lack of the transformer, TI topologies are more efficient, but at present, all the semiconductor devices used hard-switching state. There are two approaches. First topology is Zero Current-Transition (ZCT) presented in Fig. 23. Secondly, the introduction of two resonant tanks for the main high-frequency switches of the inverters uses the zero-current turn-off and zero-current turn-on for auxiliary switches [39].

Despite the high efficiency of the TI topologies over the transformer inverter topologies, the switches used the hard-switching state. New concept is known as the zero-voltage transition (ZVT). The zero-current turn-on of the auxiliary switches and zero voltage switches between the turn-off and turn-on of the high-frequency main switches and the zero-voltage turn-on and turn-off of the antiparallel diodes of the line-frequency switches are created by using two resonant tanks (Fig. 24) [40].





HERIC topology is based on the full-bridge method and has an extra bidirectional switch on the AC side for separating the gird and PV inverter throughout the freewheeling time. The bidirectional switch is made up of the two switches and the anti parallel diodes. As other full bridge methodologies, such as H5, HERIC topology also requires high filtering efforts. This effort is necessary to filter the ripple effect in the current. Output voltage and common voltage of HERIC topology is shown in Fig. 25 A and B. Due to the unipolar voltage across the filter, there are low core losses, and low leakage is achieved as well VPE [41-42].



Fig. 25 (a) Output voltage of HERIC inverter.



Fig. 25 (b) Common mode voltage of HERIC inverter.

V. NEUTRAL POINT CLAMPED (NPC) TI CONFIGURATIONS

Apart from the solutions discussed above, another form is to utilize the half-bridge inverter in which the neutral line linked to the midpoint of the dc bus as shown in Fig. 26. As we can see by using this approach, by the DC bus capacitor, we can clap the voltage across the capacitor to be unchanging, but this technique has a disadvantage which requires double DC bus voltage as compared to the full-bridge topologies.

In each switch module, a single power switch is used in Conventional single-phase full-bridge inverter topology. In the inverter, if only N-NPCC or one P-NPCC is used, during the freewheeling period, the goal of connecting both negative and positive terminal of PV array of the utility grid is not attained. So, in phase A and Phase B, two NPCCs should be employed. The rest of the power switches should be used as well [43-44]. After doing this, it creates a new family of single-phase transformerless full-bridge NPC inverters shown in Fig. 27.



Fig. 26. NPC TI Configuration 1.

Because the two-level inverter has lower performance as compared to the multilevel inverters, multilevel inverters are preferred for the use of medium voltage high power applications due to its performance. Out of multiple multilevel inverters, for PV grid connected system, the neutral point clamped multilevel inverter (NPC-MLI) is preferred. In TI Split Inductor MLI (SI-MLI) in gridconnected PV system applications, the main problem is to eliminate the leakage current, and the challenge is to keep the constant common mode voltage while eliminating the leakage current. Hysteresis Current Control (HCC) provides a very efficient solution in current control performance for SI-NPC-MLI (Fig. 28). Its performance depends on the hysteresis Band value (h) and the error current value (Δi) produced between SI-MLI and grid [45-47].



Fig. 27. Transformerless full-bridge NPC Inverter Topology PN-NPC.

The topology of HB-NPC is dissimilar to the topologies of H6 and H5, and is not comprised of the full bridge concept. HB-NPC topology is half bridged and consists of 2 clamping diodes: D4 and D6, and of 4 switches: S1, S2, S3, S4. These are connected by counterpoint of DC-Link capacitance to the neutral grid terminal.

The diode's voltage limit which is imposed on the connected switches is half of PV input voltage. From this, we can conclude that NPC topology requires two times PC input voltage as compared to the other full bridge strategies. The current produced by NPC has ripples which are equivalent to the frequency of switching. Moreover, it needs extra effort for filtering. Due to unipolar voltage, the core losses are very low across the filter [48-50].



Fig. 28. NPC TI Configuration 2.

NPC topology has its drawback despite providing an efficient solution and almost zero presence of the switching frequency ground leakage current (Fig. 28). The drawback is that it needs double DC bus voltage to produce the same output voltage which is equal to the full-bridge-based topologies. Moreover, power losses are not divided properly among the different power devices. Considering that this double DC bus voltage is not a problem for our usage and application, the NPC is the simplest, reliable and cost-effective solution. It allows us to use the transformerless power system with simple modulation, high efficiency, and excellent controllability [51-54].

To obtain Active NPC (ANPC) topology, all we need is to replace the fixing diodes D1 and D2 with active switches (Fig. 29). It is more efficient than the normal NPC, and its inverter can deliver the reactive power as well. Moreover, PWM strategies can also be incorporated depending upon the degrees of freedom with which this topology has to offer from the traditional NPC. There is a solution

in which we can double converter's output voltage switching frequency without affecting power losses. Smaller filter inductor can be used by following this approach [55-57].



Fig. 29. Active NPC TI Configuration 3.

In [58-59], a comprehensive comparison is performed between the many NPC-based PV converters and the Hbridge-based converters. The main purpose of the designing different topologies is to optimize reliability and the efficiency by considering the energy production versus the lifetime of the system and the geographical location as well (Fig. 30). In cost-effectiveness and efficient, NPC-based architectures are the best ones.



Fig. 30. Active NPC TI Configuration 4.

The GP inverter family consists of the doubly grounded inverters. In this inverter, the negative pole of the PV source is grounded. The voltage Vp is like the DC source voltage while the Voltage Vn is equal to zero. The main problem with this approach is that the output current has discontinuous waveform and it requires larger filter capacitor, Fig. 31 shows the new circuits which solve the problem mentioned above, and it was proposed in the [60-65], adding more switches decreases the efficiency and effectiveness of the system. The robustness of the total system is decreased as well.



Fig. 31. Active NPC TI Configuration 5.

Fig. 32 indicates the power circuit for the one-phase leg of a five-level NPCMLI [66-67]. SPWM (sinusoidal pulse width modulation), which is a modulation technique based on the phase disposition (PD). Amongst the existed multicarrier SPWM schemes, it ensures the best harmonic profile [68-69]. For attaining each voltage level in NPCMLI, there is only one switching strategy, and it is also the reason that there is an unequal current loading of semiconductors.



Fig. 32. Five-Level NPCMLI.

A new design technique is presented for optimizing the switching frequency and structure of the output filter (either LCL- or LLCL-type) in transformerless H5 and Coenergy-neutral point clamped (Co-energy-NPC) PV inverters, which employ SiC-type power devices (Fig. 33 and 34). The design results show that the optimized SiCbased H5 and Co-energy-NPC transformerless PV inverters are more effective regarding energy production than their non-optimized and silicon (Si)-based counterparts [70-71].



Fig. 33. Conergy-NPC1.



Fig. 34. Conergy-NPC2.

VI. COMPARATIVE STUDY

Table I shows the efficiencies of the ZVT-HERIC, ZVT-H6, and HS-HERIC as a function of the output power. It is worth to point out that the resonant parameters of the ZVT-H6-I are in accordance with the ZVT-HERIC in order to achieve 3-kW power output with optimized design. We can see from Table I that the soft switching technique is able to improve the conversion efficiency compared with hard switching one; meanwhile the ZVT-HERIC is superior to ZVT-H6-I because of the conduction loss.

Table 1: Comparative Study on Hard Switching and Soft Switching.

Output Bower	Efficiency in %				
Output Power in W	HS- HERIC[68]	ZVT- H6[37]	ZVT- HERIC[67]		
500	92.6	92.3	94.4		
750	94.3	95.2	96.4		
1000	94.8	96.6	96.6		
1250	95	96.2	97.3		
1500	95.2	96.8	97.5		
1750	95.2	97	97.35		
2000	95.4	97	97.7		
2250	95.2	96.95	97.75		
2500	95.4	97	97.8		
2750	95.3	97.1	97.8		
3000	95.4	97	97.8		

In order to evaluate the lossless advantage of proposed Switching Loss Free (SLF) concept quantitatively, the semiconductor losses of several topologies have been calculated. They include the H6-I [72], ZCT H6-I [39] and SLF H6-I [73], and the detailed data presented in Fig. 35.

The SLF-H6-I is with the least semiconductor device losses, and its switching loss and reverse recovery loss are zero. For this reason, the total semiconductor losses of the SLF-H6-I are able to be independent of the switching frequency. Therefore, the lossless advantage will be getting more outstanding as the switching frequency increases [74-75].



Fig. 35. Loss Comparison of Topologies.

All the topologies have almost same European efficiency with a slight variation because of high performance freewheeling diode of the H6-5 and H6-2 topologies. The experimental performance comparisons for these three topologies are summarized in Table 2.

It can be seen that the proposed topology can combine the superior performance of DM and CM characteristics.

 Table 2: Performance Comparison of Topologies.

Parameters	Topology 5 (Fig.14)	Topology 2(Fig.11)	Topology 4 (Fig.13)
PWM pattern	Semi- unipolar		
Leakage Current mA	24.5	26.2	19.6
THD in %	4.6	4.3	1.7
Efficiency in %	97.31	97.39	97.22

In order to calculate the power device losses, the IGBTs are evaluated by STGW20NC60VD with very soft ultrafast recovery anti parallel diode. MOSFETs and diodes have been selected with the model no SPW47N60C3 and IDH08SG60C with no reverse recovery, respectively. The total power device losses at different output power for the H5, HERIC, H6-I and H6-II are calculated under the same condition by extracting the parameters from the datasheet of the selected devices, which are given in Fig. 36. The calculation process and the theories are studied in details in the literature [8, 10, 23, 29].

The efficiency of the H5, HERIC, oH5, H6, and proposed topologies are measured for power up to 2 kW and compared is shown in Table III. The precision power analyzer is used to measure the efficiency of the proposed inverter. It is obvious that the efficiency of the proposed topology at low power (<1200 W) is highest. This is due to low-freewheeling loss compared to the other topologies. However, at 2kW, the efficiency of the HERIC topology is higher than the proposed topology which is due to the increased conduction loss.



Fig. 36. Total Device Power Loss.

measured at 600 W and found to be 98.5%. It is clear that the lowest efficiency is measured with the H6 topology. On the other hand, H5 topology ensures almost same efficiency which is lower than HERIC and proposed topologies but exceeding H6 topology.

Table 3: Comparative Study on Efficiency.

Output	Topology			
Power in W	H5[1]	HERIC [2]	H6[23]	Proposed in [10]
200	96.075	97.295	95.563	97.88
400	97.59	97.956	97.151	98.346
600	98	98.3	97.568	98.519
1000	97.939	98.426	97.671	98.5
1500	97.75	98.481	97.53	98.384
2000	97.659	98.365	97.293	98.244

The fixed voltage conduction losses of the IGBT's used in the H5 inverter are avoided in the H6 inverter topology which improves the efficiency. However, there are higher conduction losses due to the three series connected switches in the current path during active phases. The shoot-through issues due to three active switches which are series connected to the DC bus still remains in the H6 topology. Another disadvantage in the H6 inverter is that when the inverter output voltage and current has a phase shift the MOSFET body diodes may be activated. This can cause body diode reverse recovery issues and decrease the reliability of the system.

The main issue of dual-parallel-buck topology is that the arid is directly connected by two active switches, which may cause a grid short circuit problem, reducing the

The maximum efficiency of the proposed topology is reliability of the topology. A dead time of 500 µs between the two line frequency switches at the zero crossing instants needed to be added to avoid grid shoot-through. This adjustment to improve the system reliability comes at the cost of high zero crossing distortion for the output grid current. So a new TI has to be designed to overcome these problems.

H5 configuration is patented by SMA solar technology AG, used in their SUNNY BOY 2100TL series of TI's which are giving maximum efficiency of 96%. Solar edge single phase inverters of SE2200 - SE6000 series are efficiency of 97.6%. HERIC maximum giving configuration is patented by Sunways, used in their NT series of inverters which are giving maximum efficiency of 97.8%. Danfoss company TLX inverter series are giving maximum efficiency of 97.8% for 6 kW, 97.9% for 8 kW loads.

According to the above analysis, a comparison among various transformerless topologies has been conducted and summarized in Table 4. It can be seen that most of the topologies under zero- state mid-point clamped and solidity clamped methods need to be implemented with two input capacitors that can increase the complexity of the control circuit. However, these topologies present very low leakage current. In contrast, though zero-state decouple topologies cannot completely eliminate leakage current but only one input capacitor is required for them. It can be seen that some of the topologies could be implemented with less number of switches and also low voltage rating switches. The Table 6 provides the detailed analysis about the different TI topologies.

Parameters	H5	H6	HERIC	Active NPC	Conergy NPC
Maximum Possible Efficiency in %	98.5	97.4	98.3	97.34	97.67
Input Voltage Range	DC supply 400V	DC supply 400V	DC supply 400V	DC supply 800V	DC supply 800V
No. of Capacitors	1	2	1	2	2
Level of Capacitance	Small	Small	Small	Big	Big
No. of Devices	5	6	6	6	4
No. of Diodes	None	2	3	None	None
Voltage Levels Produced	3	3	3	3	3
Harmonic Content	2 FSW	2 FSW	2 FSW	2 FSW	2 FSW
Inference Problems	Less	Less	Less	Less	Less
Leakage Current	Very Less	Less	Less	Less	Less

Table 4: Comparative Study of Different Topologies.

Inverter Topology	Advantages	Disadvantages	Semiconductor	Efficiency
Half Bridge Inverter	Eliminate the leakage current with simplified configuration	DC link voltage>> Peak voltage Cost high	Switch – 2, Inductor - 1	98.3%
Dual Buck Inverter	Shoot through problems avoided	DC link Voltage high Power density issues	Buck converter 2 inductor, 2 switch, 2 capacitor 2	95%
Virtual DC Bus Based inverter	Max current stress is limited 3 times of half bridge inverter	Need to use switched capacitor	inductor, 1 switch,4 diode, 4 capacitor 2	96.6%
AC based Decoupling	Common mode voltage constant. Conduction loss less	Additional leakage Current	Switch 6 Diode 2 Inductor 2 Capacitor 1	97.8%
HERIC Inverter	High efficiency, Cost Effective	High Frequency resonance Additional leakage Current	Switch 6 Diode 2 Inductor 2 Capacitor 1	97.1%
HERIC Based Clamping Inverter	Leakage Current eliminated. Common mode voltage is flat without high frequency pulse	Cost high Power density issues	Additionally 2 Passive diode	97.8%
H5	Isolation, CM voltage constant, Leakage current less.	Ripple Current, require high filtering, fixed voltage conduction loss	Switches 5	98%
H6	Leakage current low, Low Output AC Distortions	Reliability decreased, conduction losses more. Shoot through issues	Switches 6	97.4%
HERIC	High efficiency, Isolation.	Variable CM voltage, High Leakage current in low efficiency	Switches 6	98.43%
NPC	Efficiency high, reliable, controllable	Two times PC input Voltage, Ripple Current, require high filtering	Switches 6	97.34%

VII. CONCLUSION

In this review paper, a complete evaluation of the PV system based the single-phase TI circuit configurations has been presented. The working principle, rewards, and drawbacks of the existing TI topologies available in the literature have been discussed in detail. Different categorization like ZVS and ZCS based inverters, MOSFET and IGBT based topologies are compared in this review. Efficiency comparison among H5, H6, HERIC and NPC circuits are presented. A deep conversation has been offered to pick up an appropriate topology circuit configuration among the different circuits presented in the paper. Hence, it is predictable that this research assessment will be a useful guide on PV based TI inverter for the researchers those who working on PV based systems.

Most of the PV systems are designed with transformer for safety purpose with galvanic isolation. However, the transformer is big, heavy and expensive and also it reduces the overall efficiency to (4-6) %. To overcome these problems, transformerless PV system is introduced, which is smaller, lighter, cheaper and higher in efficiency. The efficiency and reliability of single phase PV inverter systems can be improved using transformerless topologies, but new problems related to safety, leakage current arises. So, a highly reliable and efficient inverter for transformerless PV grid connected power generation systems to be designed, analyzed and tested. The following characteristics of the TI must be ensured by the researcher in future,

- No shoot through issue which leads to greatly enhanced reliability.

- Low AC output current distortion to be achieved because dead time is not needed at PWM switching commutation instants and grid cycle zero crossing instants.

 Higher switching frequency operation must be allowed to reduce the output current ripple and the size of passive components. Proper grounding the frame of the PV array reduces the capacitance; thereby the ground leakage current will be minimized.

 By carefully choosing the topology and the modulation strategy, the voltage fluctuations between the PV array and ground will be reduced.

VIII. FUTURE SCOPE

The readers may implement this work in hardware with remote monitoring and control by using suitable artificial intelligence technique.

Conflict of Interest. The authors declare no conflict of interest associated with this work.

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